



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,840	03/06/2002	Toshihiro Saika	03500.016259	5736

5514 7590 09/13/2005

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER

LAM, HUNG H

ART UNIT	PAPER NUMBER
----------	--------------

2615

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,840	SAIKA, TOSHIHIRO	
	Examiner	Art Unit	
	Hung H. Lam	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 06/15/05, have been entered and made of record. Claims 1-7 are pending.
2. In view of Applicant's amendment to Fig.1, and the title, objections to Fig. 1 and the title are hereby withdrawn.

Response to Arguments

3. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
5. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terada (US-6,124,888).

Regarding **claim 1**, Terada discloses an image processing apparatus comprising:
a sensor (Fig. 4) including a plurality of pixels each including a light receiving element (Fig. 1; diode D), and a scanning circuit (Fig. 4; horizontal 5/ vertical 7A scanning circuit) for

reading out signals in time sequence from the plurality of pixels (Col. 9, Ln. 40-50; it is inherent that the horizontal 5/ vertical 7A scanning circuit read out image signals in time sequence); and

a drive circuit, which supplies pulses for driving said scanning circuit (Fig. 7; Drive circuit 109; Col. 12, Ln. 11-18).

wherein said drive circuit (Fig. 7; 109) is so arranged to output at least a first pulse (Fig. 6A; first pulse is interpreted as the wide pulse in $\Phi V1$) and a second pulse smaller than the first pulse (Fig. 6A; second pulse is interpreted as the narrow pulse in $\Phi V1$), and said drive circuit supplies the first pulse to said scanning circuit when a first resolution is selected (Col. 9, Ln. 60-67; Figs. 6A-F, when pulse $\Phi V1$ and ΦSRn are high and then $\Phi V1$ goes low at horizontal blanking {HBL} while ΦSRn is still high, a complete line of pixels is read out).

Terada teaches a condition wherein the second pulse is $\Phi V1$ within HBL and the selection signal ΦSRn only maintains at high within HBL and goes low, which results in skipping a lines of pixels when a lower resolution is selected (Col. 8, Ln. 35-43; Col. 9, Ln. 50-67; Col. 11, Ln. 15-28).

However, Terada fails to explicitly disclose that the drive circuit supplies the first pulse and the second pulse to said scanning circuit so that the first pulse is applied to a pixel to be read out and the second pulse is applied to a pixel to be thinned out.

In an embodiment of Fig. 26, Terada teaches a so-called XY address image sensor system which can read out the signal by selecting a pixel at any optional position out of the plurality of pixels (Col. 25, Ln. 64- Col. 26, Ln. 1-5). Terada further teaches a horizontal scan register driving plurality of switches (Fig. 26; SW1-SW6) to control the readout signal (Col. 26, Ln. 30-33). Additionally, Terada teaches that the output Bayer layout of the image sensor may be

thinned out to $\frac{1}{4}$ both horizontally and vertically (col. 26, Ln. 44-56). In light of the teaching from this embodiment, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Terada by having the drive circuit supplies pulses to the scanning circuit, which control the switches to read or not to read (thin out) a pixel at any optional position out of the plurality of pixels in order to provide an improve image sensor wherein any pixel position are addressable for reading out or thinning out by scanning pulses.

Regarding **claim 2**, Terada discloses an apparatus wherein when the second resolution is selected, said drive circuit supplies the first pulse in every other pulse or in every plurality of pulses (Fig. 6A; Col. 8, Ln. 35-43; second resolution is selected and only odd lines $\Phi SR1$ and $\Phi SR3$ are selected for reading out; scanning circuit is provided with the wide pulse $\Phi V1$ in every other narrow pulse {within HBL}; see Fig. 6A).

Regarding **claim 3**, Terada further discloses an apparatus comprising a signal processing circuit which performs image processing on the basis of signals which are read out by supplying the first pulse to said scanning circuit (Col. 9, Ln. 55-67; Figs. 6A-F; the wide pulse in $\Phi V1$ is interpreted as the first pulse; it is noticed that when pulse $\Phi V1$ and ΦSRn are high and then $\Phi V1$ goes low at HBL while ΦSRn is still high, a complete line of pixels is read out).

Regarding **claim 4**, Terada discloses an apparatus as recited in the rejection of claim 2. However, Terada fails to explicitly disclose that the sensor is formed on the same semiconductor chip, and a plurality of said sensors are mounted on a mount board.

However, the examiner takes Official Notice that it is well known and expected in the art for forming image sensors on the same semiconductor chip and mounting sensors on a printed circuit board. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image processing apparatus of Terada by forming the sensors on the same semiconductor chip and mounting them on the board in order to provide a wide dynamic range image sensor having a compact structure.

Regarding **claim 5**, Terada discloses an apparatus wherein each of said pixels has an amplifying device which amplifies a signal from the light receiving element, and which outputs the amplified signal (Fig. 4; Col. 8, Ln. 44-50; Terada teaches an amplification type solid-state imaging device; additionally, it is commonly known in the art that each pixel/ light receiving element is included with a transistor/ amplifier device for amplifying an image signal), a reset switch for resetting an input portion of said amplifying device (Col. 9, Ln. 1-10; it is inherent that the image sensor is included a reset switch in order for the reset voltage VRS to reset the input switch), and a selecting switch (Fig. 4, SW3) for selectively reading the signal from said amplifying device (Col. 9, Ln. 10-13), said selecting switch being supplied with a pulse from said scanning circuit (Col. 9, Ln. 10-15; Col. 9, Ln. 40-67).

Regarding **claim 6**, Terada further discloses an apparatus comprising a control circuit (Fig. 7; system controller 108) for switching between the first resolution and the second resolution (Col. 12, Ln. 11-29).

Regarding **claim 7**, Terada discloses an apparatus as recited in claim 1. However, Terada fails to disclose a light source for irradiating light on said sensor, and a transport member for moving an original and said sensor relative to each other.

However, the examiner takes Official Notice that it is well known and expected in the art for providing a light to irradiate on a reading surface and a transport member for moving the sensor and an original relative to each other. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image processing apparatus of Terada by having an irradiating light and a transport member in order to provide a scanner having adequate illumination.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

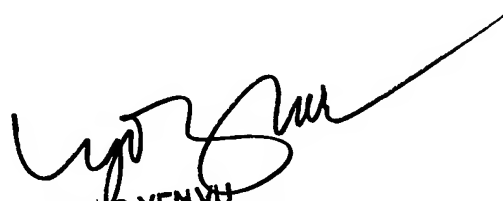
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on 571-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HL

09/06/05


NGOC-YEN VU
PRIMARY EXAMINER